1.General Description

This OTP-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 3K words of EPROM, and 128bytes of static RAM.

2.Features

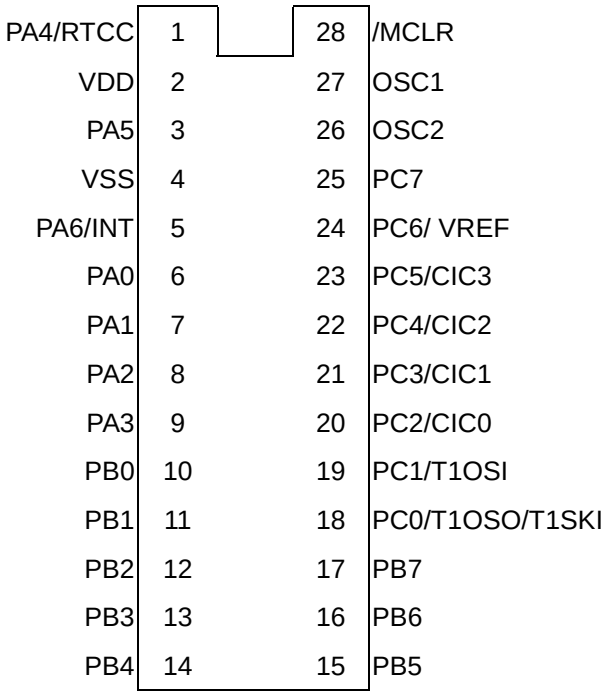
- RISC CPU
- Fully static design
- 37 single word instructions
- 3K × 14 program memory
- 128 bytes RAM for data
- 23 bi-directional I/O
- Eight level hardware stacks
- Watchdog timer (WDT) with on-chip RC oscillator
- Power-On Reset (POR) ,only available while PED is Disable
- Power Edge-detector Reset (PED)
- Interrupt capability
- Timer0:8-bit timer with 8-bit prescaler (RTCC)
- Timer1:16bit timer with 16bit compare register. This timer can be used as carrier generator.
- 4 Channel comparator
- Sleep mode for power saving.
- PB with port change wake- up interrupt

3.Applications

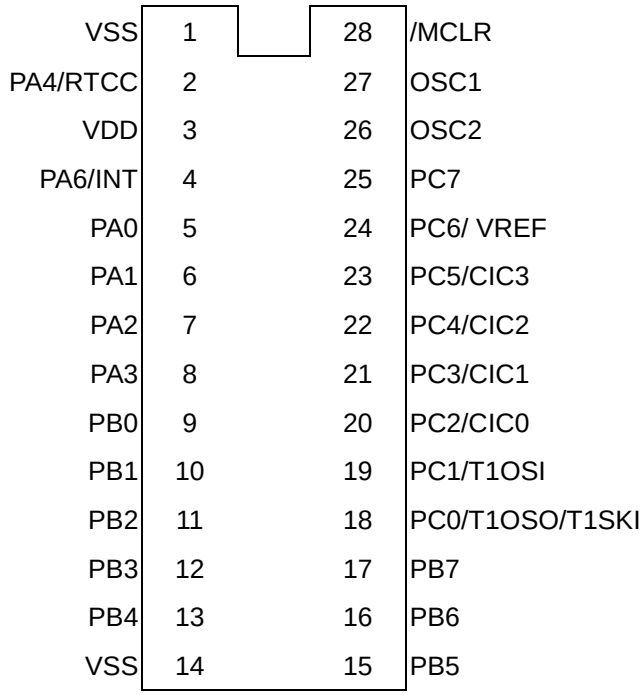
The application areas of this NEW MCU range from appliance motor control and high speed automotive to low power remote transmitters/receivers and telecommunications processors, such as Remote controller, small instruments, toy , automobile and keyboard…etc.

4. *Pin Diagram*

DIP/SOP



SSOP



5. Pin function description

Pin name	Type	Buffer type	Description
OSC1	I		Oscillator input
OSC2	O		Oscillator out
/MCLR	I	ST	Reset input
			Bi-directional I/O port A. PA6 internal pull-high 80K ohm
PA0	I/O	TTL	
PA1	I/O	TTL	
PA2	I/O	TTL	.
PA3	I/O	TTL	
PA4	I/O	ST	PA4 Can be clock input to RTCC input
PA5	I/O	TTL	
PA6(/INT)	I/O	ST/TTL	Can be change pin function to be external interrupt pin /int
			Bi-directional I/O port B. Port B can be software programmed for internal 100K ohm pull-up on all pins. PB0-PB7 can generate interrupt on pin state change.
PB0	I/O	ST/TTL	PB0 serial programming clock
PB1	I/O	ST/TTL	PB1 serial programming data
PB2	I/O	TTL	
PB3	I/O	TTL	
PB4	I/O	TTL	
PB5	I/O	TTL	
PB6	I/O	TTL	
PB7	I/O	TTL	
			Bi-directional I/O port C..
PC0	I/O	ST	Can be Timer1 oscillator output or Timer1 clock input.
PC1	I/O	ST	Can be Timer1 oscillator input.
PC2	I/O	TTL	TTL input level or Comparator input
PC3	I/O	TTL	TTL input level or Comparator input
PC4	I/O	TTL	TTL input level or Comparator input
PC5	I/O	TTL	TTL input level or Comparator input
PC6	I/O	TTL	TTL input level or Comparator VREF input
PC7	I/O	TTL	
Vdd			Power input
Vss			Ground pin

6. Memory Mapping

6.1Program memory :

0000h	Reset Vector
0001h	
0002h	
0003h	
0004h	Peripheral interrupt Vector
0005h 07FFh	Program memory (Page 0)
0800h 0BFFh	Program memory (Page 1)

6.2Register file map :

	BANK 0	BANK 1	
00h	IAR	IAR	80h
01h	RTCC	TMR	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	MSR	MSR	84h
05h	PORT A	CPIO A	85h
06h	PORT B	CPIO B	86h
07h	PORT C	CPIO C	87h
08h			88h
09h			89h
0Ah	PCHLAT	PCHLAT	8Ah
0Bh	INTS	INTS	8Bh
0Ch	PIFB1	PIEB1	8Ch
0Dh			8Dh
0Eh	TMR1L	PSTA	8Eh
0Fh	TMR1H		8Fh
10h	T1CON	OPTION2	90h
11h			91h
12h			92h
13h			93h
14h			94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCPR1C		97h
18h 1Fh			98h 9Fh
20h 7Fh	General Purpose Register	General Purpose Register	A0h BFH

Unimplemented memory location.

BANK0

00 IAR (Indirect addressing register)

01 RTCC (Timer0) register

02 Program counter low byte

03 Status register

Bit	Symbol	Function
0	C	Carry
1	DC	Digit carry
2	Z	Zero flag
3	PF	Power-down flag
4	TF	WDT time-out flag
5	Bank	Register bank select (For direct addressing) =0 Bank 0 (00h-7Fh) =1 Bank 1 (80h-BFh)
6:7		General purpose bit

04 MSR (Memory select register)

05 PORTA (Port A data register)

06 PORTB (Port B data register)

07 PORTC (Port C data register)

08 Unimplemented.

09 Unimplemented.

0A PCHLAT (Program memory segment register)

0B INTS (Interrupt control register)

Bit	Function
0	PB port change interrupt flag bit.
1	/INT external interrupt flag bit.
2	RTCC(Timer0) overflow interrupt flag bit.
3	PB port change interrupt enable bit.
4	/INT external interrupt enable bit.
5	Timer0 overflow interrupt enable bit.
6	Peripheral interrupt enable bit.
7	Global interrupt enable bit.

0C PIFB1 (Peripheral interrupt flag register 1.)

Bit	Function
0	Timer1 overflow interrupt flag bit
7-1	Unimplemented. Always read as 0.

0D Unimplemented.

0E TMR1L (Timer1 data register low byte.)

0F TMR1H (Timer1 data register high byte.)

10 T1CON (Timer1 control register)

Bit	Function
0	Timer1 enable bit (0:disable 1:enable)
1	Timer1 clock source select (0:internal clock 1:external input)
2	Timer1 external clock synchronization control bit (0:synchronization 1: asynchronous)
3	Timer1 oscillator enable control bit (0:disable 1:enable)
4-7	Unimplemented. Always read as 0.

11-14 Unimplemented.

15 CCPR1L (Timer1 compare low register.)(8BIT)

16 CCPR1H (Timer1 compar high register.)(8BIT)

17 CCPR1C (Timer1 compare control register)

Bit 7-1 –Unimplemented. Always set as 0.

Bit 0 – compare enable bit (0:disable 1:enable)

18-1F Unimplemented.

20-7F General purpose register

BANK1

80 Same as register 00.

81 TMR (Time mode register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2–0	PS 2–0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assign bit 0:RTCC 1:WDT		
4	TCE	RTCC edge select bit 0:Increment on low to high 1:Increment on high to low		
5	TCS	RTCC clock source select bit 0:Internal clock 1:RTCC Pin		

Bit	Symbol	Function
6		/INT interrupt edge select bit
7		Port B pull-up enable bit. (0:enable 1:disable)

82-84 Same as 02H-04H.

85 Port A data direction register.(CPIO A)

86 Port B data direction register.(CPIO B)

87 Port C data direction register.(CPIO C)

88 Unimplemented.

89 Unimplemented.

8A-8B Same as 0AH-0BH.

8C Peripheral interrupt control register 1.

Bit 0 – Timer1 overflow interrupt enable bit.

7-1 – Unimplemented. Always set these bits to 0.

8D Unimplemented.

8E PSTA (Power control register and Comparator control register.)

BIT	Function
0	The comparator function enable bit (0:disable 1:enable)
1	Power-on reset status bit
2	0:Define PC2 as TTL input (CMR0) 1:Define PC2 as comparator input.
3	0:Define PC3 as TTL input (CMR1) 1:Define PC3 as comparator input.
4	0:Define PC4 as TTL input (CMR2) 1:Define PC4 as comparator input.
5	0:Define PC5 as TTL input (CMR3) 1:Define PC5 as comparator input.
7:6	Reference Voltage select(CMR5~CMR4) 00: 1/4 VDD 01: 1/2 VDD 10: 3/4 VDD 11: VREF(External pin and PC6 must set to input)

8F Unimplemented.

90 Option register 2. (“ 0 ” Enable ; “ 1 ” Disable)

Bit 0–3 5–7 : Unimplemented.

4 – PA 6 pull-up enable bit.

91-9F Unimplemented.

A0-BF General purpose register.

7.Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h(80h)	0000 0000	0000 0000	uuuu uuuu
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h(82h)	0000 0000	0000 0000	0000 0100
STATUS	03h(83h)	0001 1xxx	000# #uuu	000# #uuu
MSR	04h(84h)	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT C	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCHLAT	0Ah(8Ah)	---- 0000	---- 0000	---- uuuu
INTS	0Bh(8Bh)	0000 0001	0000 0001	uuuu uuuu
PIFB1	0Ch	---- ---x	---- ---u	---- ---u
TMR1L	0Eh	xxxx xxxx	Uuuu uuuu	Uuuu uuuu
TMR1H	0FH	xxxx xxxx	Uuuu uuuu	Uuuu uuuu
T1STA	10h	---- 0000	---- 0000	---- uuuu
CCP1L	15h	xxxx xxxx	uuuu uuuu	--uu uuuu
CCP1H	16h	xxxx xxxx	Uuuu uuuu	--uu uuuu
CCP1CTL	17h	---- ---0	---- ---0	---- ---u
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	1111 1111	1111 1111	uuuu uuuu
CPIOB	86h	1111 1111	1111 1111	uuuu uuuu
CPIOC	87h	1111 1111	1111 1111	uuuu uuuu
PIEB1	8Ch	---- ---0	---- ---0	---- ---u
PSTA	8Eh	0000 00#0	0000 00u0	0000 00u0
OPTION2	90h	---1 ----	---1 ----	---u ----

Note ： u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”

#＝value depends on the condition of the following table

Condition	Status bit 4	Status bit 3	PSTA bit 1
POWR ON RESET	1	1	0
/MCLR reset (not during SLEEP)	u	u	u
/MCLR reset during SLEEP	1	0	u
WDT reset (not during SLEEP)	0	1	u
WDT reset during SLEEP	0	0	u
Interrupt Wake-up during SLEEP	1	0	u

8. *Instruction Set*

Instruction Code	Mnemonic Operands	Function	Operation	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔ R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R －W→t (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R －1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R －1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z

Instruction Code	Mnemonic Operands	Function	Operation	Status
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n)→R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110001 iiiiiiii	RTIW i	Return, place immediate to W	Stack→PC, i→W	None
110111 iiiiiiii	ADDWI	Add immediate to W	PC+1→PC, W+i→W	C,HC,Z
111000 iiiiiiii	SUBWI	Subtract W from immediate	i-W→W	C,HC,Z
010000 00001001	RTFI	Return from interrupt	Stack→PC, 1→GIS	None
010000 00000100	RET	Return from subroutine	Stack→PC	None

Note :

W : Working register
WT : Watchdog timer
TMODE : TMODE mode register
CPIO : Control I/O port register
b : Bit position
t : Target
0 : Working register
1 : General register

		(PA, PB, PC Only)	R	:	General register address
TF	:	Timer overflow flag	C	:	Carry flag
PF	:	Power loss flag	HC	:	Half carry
PC	:	Program Counter	Z	:	Zero flag
OSC	:	Oscillator	/	:	Complement
Inclu.	:	Inclusive ‘∪’	x	:	Don’t care
Exclu.	:	Exclusive ‘⊕’	i	:	Immediate data (8 bits)
AND	:	Logic AND ‘∩’	n	:	Immediate address

9. Electrical Characteristics

(A)Operation Voltage & Frequency

Vdd : 2.3V~6.3V

Frequency: 0Hz~20MHz

(B)Input Voltage

	Port	MIN	MAX
Vil	PA , PB	Vss	1.0V
	RTCC /MCLR	Vss	1.0V
Vih	PA , PB	2.0V	Vdd
	RTCC /MCLR	3.4V	Vdd

*Threshold Voltage

PortA PortB PortC Vth = 1.6V

RTCC,/MCLR Vil=1.2V Vih=3.1V (Schmitt Trigger)

(C) Output Voltage

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

PA, PB, PC Port	
I_{oh}＝－20.0 mA	V_{oh}＝3.8 V
I_{ol}＝20.0 mA	V_{ol}＝0.6V
I_{oh}＝－5.0 mA	V_{oh}＝4.7V
I_{ol}＝5.0 mA	V_{ol}＝0.2V

(D)Leakage Current

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

I_{il}	－ 1.0 μA (Max.)
I_{ih}	＋ 1.0 μA (Max.)

(E) Sleep Current

@WDT－Enable, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.3 V	Idd=1uA
V_{dd}＝3.0 V	I_{dd}=2.0 μA
V_{dd}＝4.0 V	I_{dd}=5.0μA
V_{dd}＝5.0 V	I_{dd}=10.0μA
V_{dd}＝6.3 V	I_{dd}=18.0μA

@WDT－Disable, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.3 V ~ 6.3 V, I_{dd}＜0.1 μA

(F) Operating Current / Voltage

Temperature＝25℃, the typical value as followings :

(i) OSC Type＝RC (OSC1&OSC2 internal CAP about 10P) ; WDT－Enable;

The IC may not oscillate properly if the resistance of rext less than 4.7K

The minimum resistance of rext must be more than 4.7K

@ V_{dd}＝5.0 V

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
3P	4.7 K	7.7M	780u
	10.0 K	4.0M	480u
	47.0 K	890K	200u
	100.0 K	425K	155u
	300.0 K	140K	135u
	470.0 K	96K	126u
20P	4.7 K	4.8M	535u
	10.0 K	2.5M	340u
	47.0 K	540K	150u
	100.0 K	265K	130u
	300.0 K	87K	126u
	470.0 K	55.6K	124u

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
100P	4.7 K	2.0M	279u
	10.0 K	1.0M	186u
	47.0 K	220K	122u
	100.0 K	103K	109u
	300.0 K	34.6K	107u
	470.0 K	22.K	88u
300P	4.7 K	850 K	365u
	10.0 K	370 K	301u
	47.0 K	90 K	270u
	100.0 K	43 K	265u
	300.0 K	15K	256u
	470.0 K	9.0 K	250u

(ii) OSC Type＝LF;(OSC1&OSC2 Internal cap)

LF WDT - disable, PED – disable

IC1:

	32K(C=50P)	455K	1M	Sleep
2.3V	4uA	20uA	29uA	<0.1uA
3.0V	8uA	37uA-	50uA	<0.1uA
4.0V	20uA	86uA	95uA	<0.1uA
5.0V	43uA	143uA	127uA	<0.1uA
6.0v	88uA	237uA	185uA	<0.1uA
6.4V	111uA	280uA	215uA	0.1uA

(iii) OSC Type=XT (OSC1&OSC2 Internal cap) , WDT - enable, PED – disable

IC1:

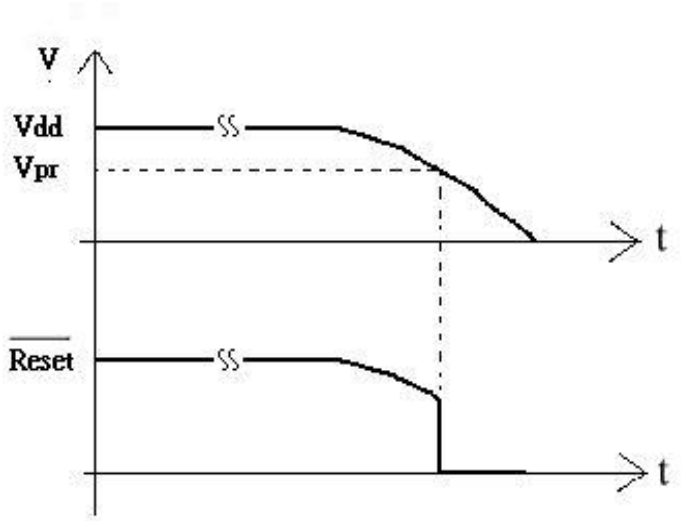
	1M	4M	10M	Sleep
2.3V	42uA	110uA	251uA	1uA
3.0V	71uA	177uA	381uA	2uA
4.0V	141uA	302uA	583uA	5uA
5.0V	314uA	460uA	869uA	10uA
6.0V	558uA	581uA	1.2mA	15uA
6.4V	702uA	760uA	1.25mA	18uA

(iv) OSC Type＝HF (OSC1&OSC2 Internal cap) WDT - enable, PED – disable

IC1	4M	10M	20M	Sleep
2.3V	106uA	288uA	---	1uA
3.0V	171uA	403uA	775uA	2uA
4.0V	353uA	682uA	1.3mA	5uA
5.0V	569uA	966uA	1.85mA	10uA
6.0V	830uA	1.4mA	2.5mA	15uA
6.4V	937uA	1.5mA	2.8mA	18uA

(G)Power Edge-detector Reset Voltage (Not in Sleep Mode) @Vdd=5.0V(PED=Enable)

V_{pr}≦1.6V~1.80V V_{pr} : V_{dd} (Power Supply)



PS: If PED_Enable then Internal Power-On Reset will be off

(H) The basic WDT time-out cycle time

@Temperature＝25 ℃, the typical value as followings :

Voltage (V)	Basic WDT time-out cycle time (ms)
2.3	26.4ms
3.0	24.6ms
4.0	22ms
5.0	20ms
6.3	19.4ms

(I) Pull_High Resistance

@ Input Mode : V_{dd}＝5.0 V

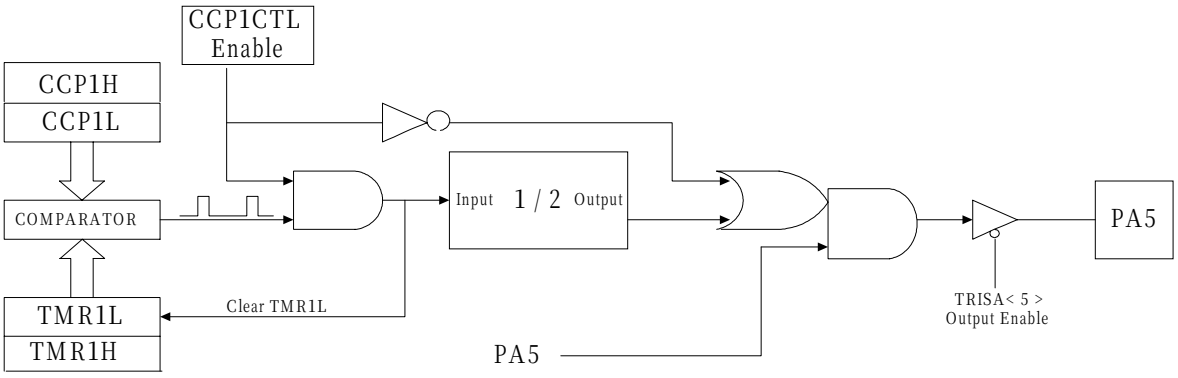
PB 7~0	PA6
5V=90k	5V=45k

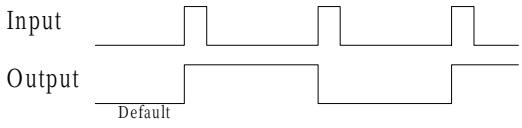
p.s. : It is only a reference value for the Pull High Resistance, and the accurate value of the Resistance depends on the various parameter of the Process. But the variation of the value will be not more than 20%.

10. TIMER1 timer/counter

1 Timer1 is a 16bit timer/counter consisting two 8-bit register (TMR1H and TMR1L) increment from 0000h to FFFFh.Timer1 can operate two mode (time mode and counter mode).Used the TICON register to control Timer1 mode

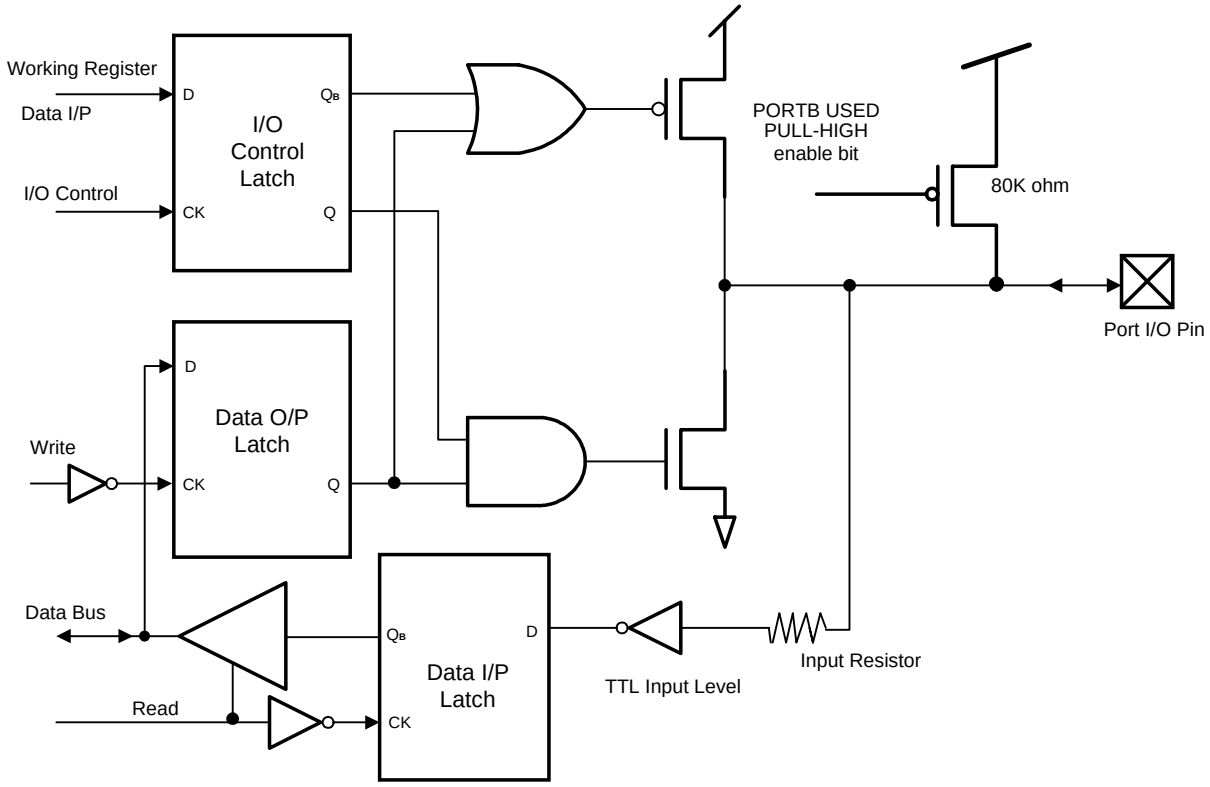
2 Timer1 ccp mode: timer1 can internal “reset “ by CCP mode,CCP register consisting two 8bit register ccp1L and ccp1H and control the register(17H-bit0) enable the comparator to reset timer1



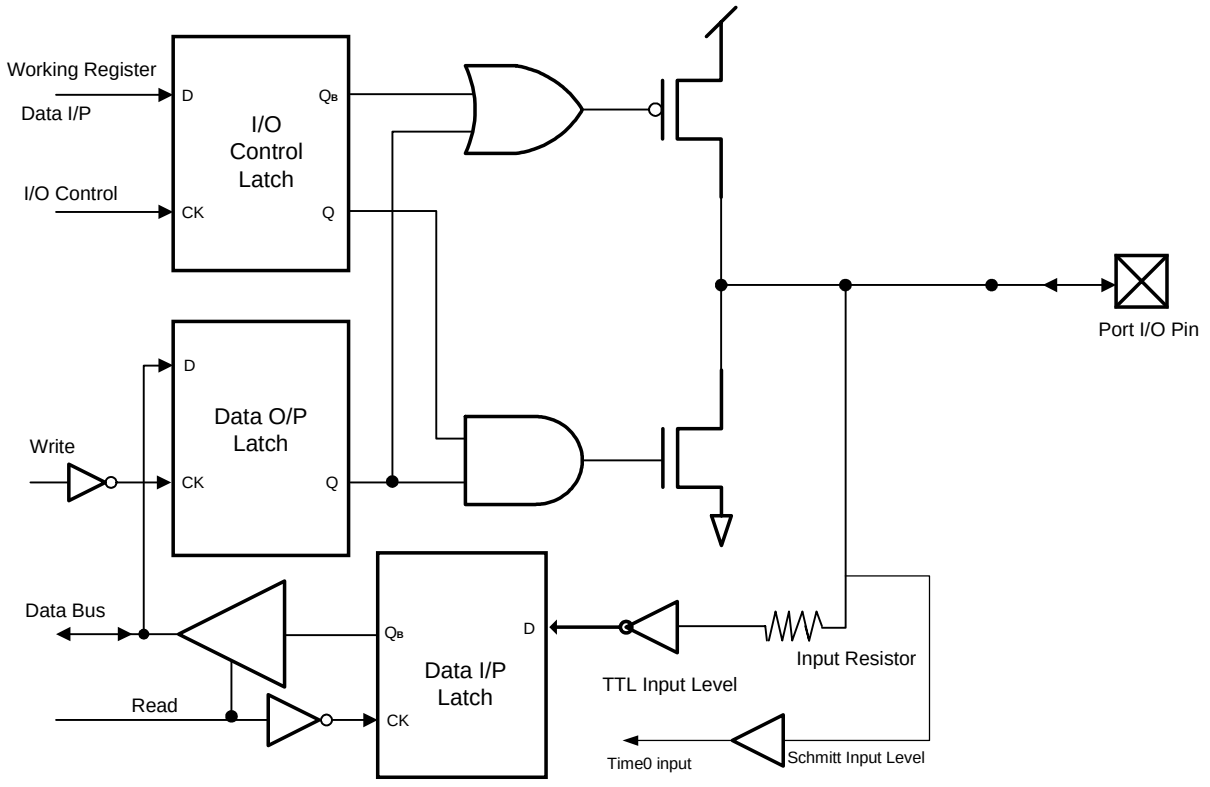


11. *Port A ,Port B and Port C Equivalent Circuit*

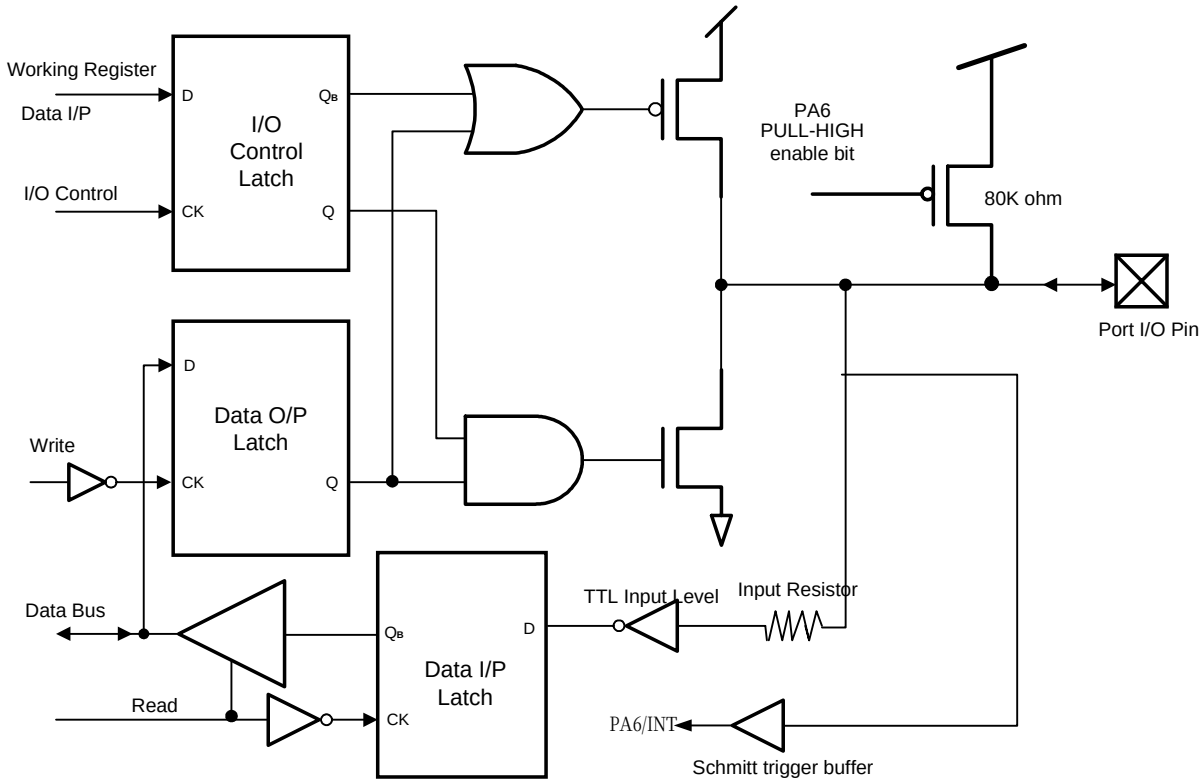
PA0~3 ,PA5 ,PB0~PB7 ,PC7



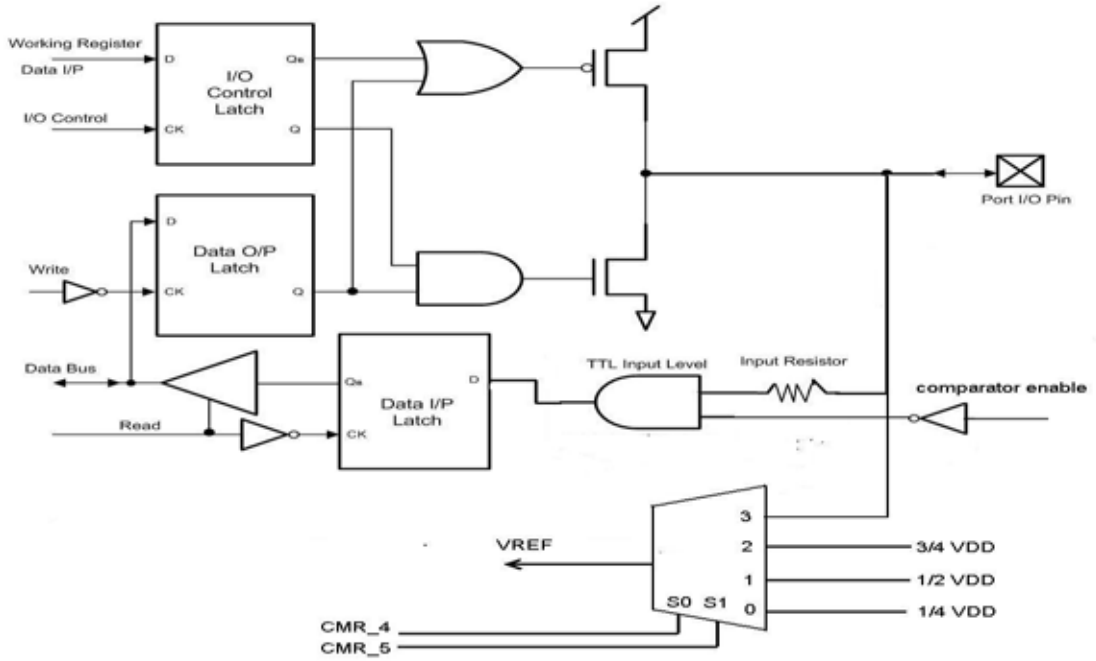
PA4/RTCC



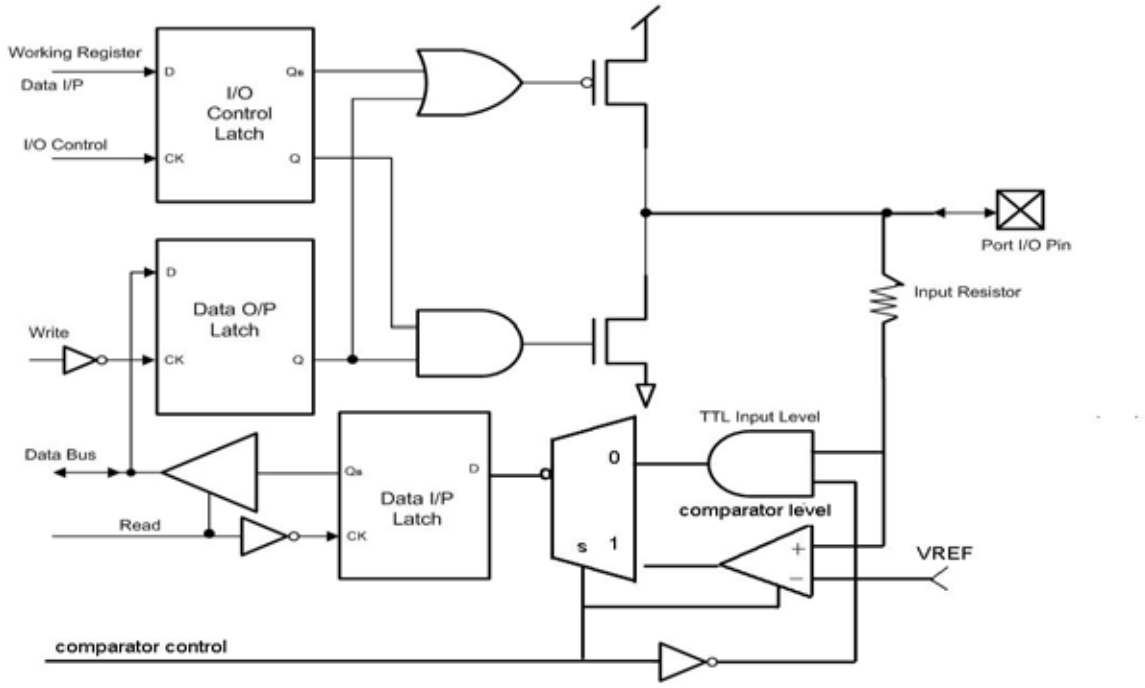
PA6/INT



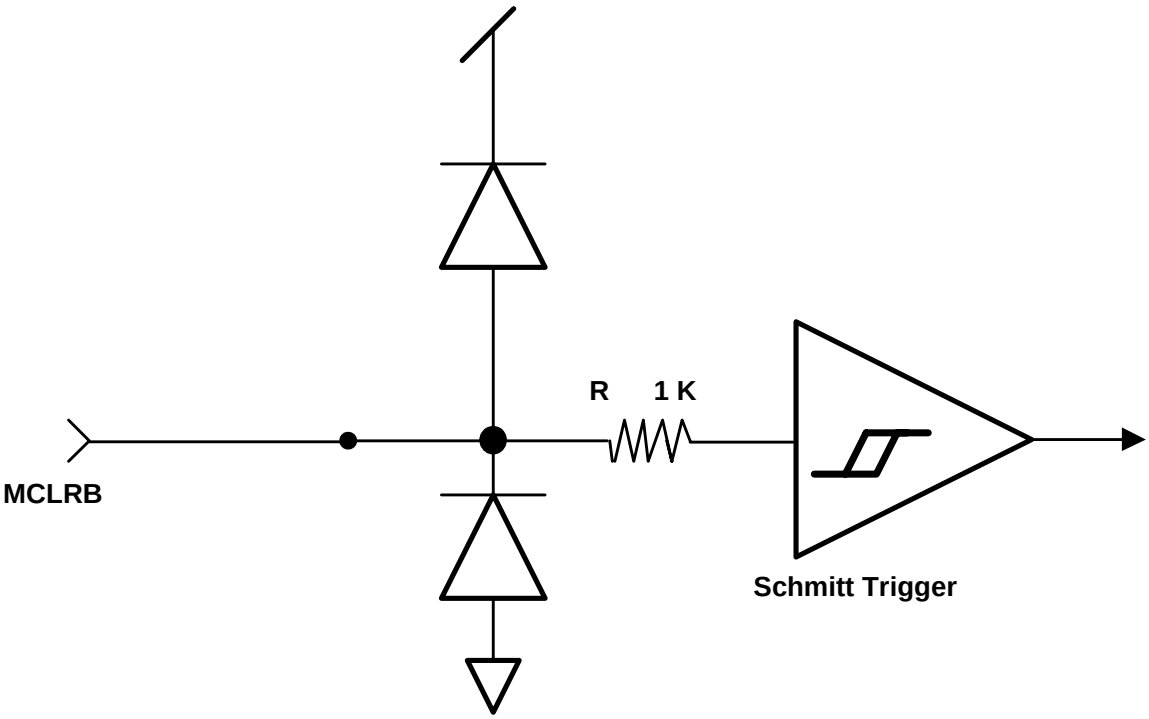
PC6/VREF



PC2~PC5



12. *MCLRB Input Equivalent Circuit*



13. Block Diagram